Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A memory device comprising:

an array of memory locations implemented as bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations; and

control circuitry coupled with the array of memory locations to cause a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations.

2. (Original) The memory device of claim 1 wherein the control circuitry causes a header having an indication of a memory location corresponding to the block of data to be stored within the first block of memory locations.

3. (Original) The memory device of claim 1 wherein the bit-alterable, non-volatile memory includes cells including a thin film chalcogenide alloy material.

4. (Original) The memory device of claim 3 wherein the chalcogenide alloy material comprises GeSbTe.

5. (Original) The memory device of claim 3 wherein the chalcogenide alloy material is selected from the group consisting of: GaSb, InSb, InSe, Sb_2Te_3, GeTe, $Ge_2Sb_2Te_5$, InSbTe, GaSeTe, $SnSb_2Te_4$, InSbGe, AgInSbTe, (GeSn)SbTe, GeSb(SeTe), and $Te_{81}Ge_{15}Sb_2S_2$.

6. (Original) The memory device of claim 1 wherein the block of data comprises system data to be used during system initialization and further wherein the block of data is stored in a pre-selected location within the memory array for all initialization sequences.

7. (Original) A method comprising:

receiving data to be stored in a bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations; and

causing the data to be stored as at least one data fragment that spans a boundary between a first block of memory locations and a second block of memory locations.

8. (Original) The method of claim 7 further comprising causing a header having an indication of a memory location corresponding to the data fragment to be stored within the first block of memory locations.

9. (Currently Amended) The method ~~device~~ of claim 7 wherein the bit-alterable, non-volatile memory includes cells including a thin film chalcogenide alloy material.

10. (Currently Amended) The method ~~device~~ of claim 9 wherein the chalcogenide alloy material comprises GeSbTe.

11. (Currently Amended) The method ~~device~~ of claim 9 wherein the chalcogenide alloy material is selected from the group consisting of: GaSb, InSb, InSe, Sb_2Te_3, GeTe, $Ge_2Sb_2Te_5$, InSbTe, GaSeTe, $SnSb_2Te_4$, InSbGe, AgInSbTe, (GeSn)SbTe, GeSb(SeTe), and $Te_{81}Ge_{15}Sb_2S_2$.

12. (Currently Amended) An article comprising a non-volatile memory ~~computer-readable medium having stored thereon~~ storing instructions that, when executed, cause one or more processors to:

receive data to be stored in a bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations; and

cause the data to be stored as at least one data fragment that spans a boundary between a first block of memory locations and a second block of memory locations.

13. (Original) The article of claim 12 further comprising instructions that, when executed, cause the one or more processors to cause a header having an indication of a memory location corresponding to the data fragment to be stored within the first block of memory locations.

14. (Currently Amended) The article ~~device~~ of claim 12 wherein the bit-alterable, non-volatile memory includes cells including a thin film chalcogenide alloy material.

15. (Currently Amended) The article ~~device~~ of claim 14 wherein the chalcogenide alloy material comprises GeSbTe.

16. (Currently Amended) The article ~~device~~ of claim 14 wherein the chalcogenide alloy material is selected from the group consisting of: GaSb, InSb, InSe, Sb_2Te_3, GeTe, $Ge_2Sb_2Te_5$, InSbTe, GaSeTe, $SnSb_2Te_4$, InSbGe, AgInSbTe, (GeSn)SbTe, GeSb(SeTe), and $Te_{81}Ge_{15}Sb_2S_2$.

17-24. (Canceled)

25. (Original) A system comprising:

an antenna;

a memory system coupled with the antenna, the memory system having an array of memory locations implemented as bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations and control circuitry coupled with the array of memory locations to cause a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations.

26. (Original) The system of claim 25 wherein the control circuitry causes a header having an indication of a memory location corresponding to the block of data to be stored within the first block of memory locations.

27. (Original) The system of claim 25 wherein the bit-alterable, non-volatile memory includes cells including a thin film chalcogenide alloy material.

28. (Original) The system of claim 27 wherein the chalcogenide alloy material comprises GeSbTe.

29. (Original) The system of claim 27 wherein the chalcogenide alloy material is selected from the group consisting of: GaSb, InSb, InSe, Sb_2Te_3, GeTe, $Ge_2Sb_2Te_5$, InSbTe, GaSeTe, $SnSb_2Te_4$, InSbGe, AgInSbTe, (GeSn)SbTe, GeSb(SeTe), and $Te_{81}Ge_{15}Sb_2S_2$.